Please amend the paragraph beginning on page 3, line 19 as follows:

In the illustrated receiver the clock and data recovery circuit 320 aligns the rising edge of the extracted clock 330 with the transition edge of the amplified data D1. In practice, however, the rising edge of the extracted clock 330 should be aligned with the equalized data (D2) output by the slicer 350 for proper data recovery by ~~flip-flop~~ flip-flop 340. Therefore, the time delay through summer 360 and slicer 350 should be equal to the time delay through buffer stage(s) 310 to ensure that the input data (D2) and clock signal 330 of ~~flip-flop~~ flip-flop 340 are aligned to properly recover the equalizer data.

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Please amend the paragraph beginning on page 5, line ~~34~~ 33 as follows:

In this embodiment, the binary signal output by the slicer 460 directly drives the data input of ~~flip-flop~~ flip-flop 470 as well as the clock and data recovery circuit 420. The clock and data recovery circuit 420 therefore generates an extracted clock signal from the binary signal (D3) output by the slicer rather than from the incoming data 440 as is done in conventional receivers (see FIG. 3). The extracted clock output by the clock and data recovery circuit 420 is then used to clock the decision feedback equalizer ~~flip-flop~~ flip-flop 470 that recovers the data from the binary signal (D3) in response to the extracted clock.

Please amend the paragraph beginning on page 6, line 11 as follows:

The clock and data recovery circuit 420 may automatically align the rising edge of the extracted clock, for example, with transitions in the binary signal (D3) output by the slicer 460. Therefore, the illustrated embodiment may maintain the proper timing relationship between the ~~flip-flop~~ flip-flop 470 drive data (D3) and clock (i.e. the extracted clock) to ensure proper data recovery without the need for additional delay matching stages. The elimination of high speed delay matching circuits reduces the power consumption and die area of the receiver.

Please amend the paragraph beginning on page 6, line 21 as follows:

In the illustrated embodiment a multiplier 480 scales the recovered equalized data output by the ~~flip-flop~~ flip-flop 470 by an equalization coefficient (g1) to generate the equalized feedback signal 450. The value of the equalization coefficient depends on the level of inter-symbol